ABSTRACT OF THE DISCLOSURE

A method for testing an emulated logic circuit is described wherein a model of the logic circuit is loaded into a hardware emulator (EM) and there put into an operating mode in which flip-flops it contains are functionally chained into one or more shift registers. The structural arrangement of the logic circuit in the hardware emulator (EM) is subsequently compared with the structural arrangement of the model of the logic circuit with the assistance of this operating mode. A device for implementing the method is also described.